Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method of forming a memory device having a self-aligned contact, comprising:

providing a substrate having a floating gate dielectric layer formed thereon;

forming a floating poly gate layer on the floating gate dielectric layer;

forming a first silicon nitride layer on the floating poly gate layer;

forming a patterned photoresist layer on the first silicon nitride layer;

etching exposed areas of the first silicon nitride layer and the floating poly gate layer using the patterned photoresist layer as an etch mask;

forming an oxide layer over the exposed etched areas;

removing the patterned photoresist layer and the first silicon nitride layer to expose the floating poly gate layer;

forming poly spaces in the floating poly gate layer; and

depositing a second silicon nitride layer over the poly spaces of the floating poly gate layer to form a self-aligned contact.

2. (Currently Amended) The method as set forth in claim 1, wherein the depositing of a second silicon nitride layer comprises depositing a second silicon nitride layer over the floating poly gate layer and the oxide layer.

3. (Currently Amended) The method as set forth in claim 1, ~~and~~ further comprising etching the first silicon nitride layer to expose a portion of the floating poly gate layer.

4. (Cancelled)

5. (Currently Amended) The method as set forth in claim 3, further comprising etching the second silicon nitride layer to create silicon nitride spacer formations.

6. (Original) The method as set forth in claim 5, wherein the silicon nitride spacer formations are formed over the floating poly gate layer.

7. (Original) The method as set forth in claim 1, wherein:

the floating poly gate layer is a first floating poly gate layer;

the method further comprises depositing a second floating poly gate layer over the first floating poly gate layer, the oxide layer, and the silicon nitride spacer formations.

8. (Original) The method as set forth in claim 7, further comprising depositing an interlayer dielectric on the second floating poly gate layer.

9. (Original) The method as set forth in claim 8, wherein the interlayer dielectric comprises an oxide/nitride/oxide stacked film.

10. (Currently Amended) The method as set forth in claim 3, wherein the etching of the first silicon nitride layer comprises a dry etch process.

11. (Currently Amended) ~~An apparatus~~ The device formed using the method of claim 1.

12. (Currently Amended) ~~An apparatus~~ The device formed using the method of claim 5.

13. (Currently Amended) ~~An apparatus~~ The device formed using the method of claim 9.

14. (Currently Amended) A method of forming a memory device having a self-aligned contact, comprising:

providing a substrate having a floating poly gate ~~feature~~layer and oxide features on source and drain sides of the floating poly gate ~~feature~~layer;

forming poly spaces in the floating poly gate layer; and

depositing a silicon nitride layer over the poly spaces of the floating poly gate ~~feature~~layer to form a self-aligned contact.

15. (Currently Amended) The method as set forth in claim 14, wherein:

the silicon nitride layer is deposited over the floating poly gate ~~feature~~layer and the oxide features; and

the method further comprises etching the silicon nitride layer to expose a portion of the floating poly gate layer.

16. (Original) The method as set forth in claim 15, wherein the silicon nitride layer is etched into silicon nitride spacer formations.

17. (Original) The method as set forth in claim 16, wherein the etching of the silicon nitride layer results in formation of silicon nitride spacer formations over the floating poly gate layer.

18. (Currently Amended) The method as set forth in claim 16, wherein the floating poly gate layer is a first floating poly gate layer and the method further comprises:

depositing a second floating poly gate layer over the first floating poly gate ~~feature~~layer, the oxide features, and the silicon nitride spacer formations; and

depositing an interlayer dielectric on the second floating poly gate layer.

19. (Original) The method as set forth in claim 16, wherein the etching of the silicon nitride layer comprises a wet etch process.

20. (Currently Amended) ~~An apparatus~~ The device formed using the method of claim 14.

21. (Currently Amended) ~~An apparatus~~ The device formed using the method of claim 16.

22. (Currently Amended) ~~An apparatus~~ The device formed using the method of claim 18.